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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/780,083	TOPHAM, NIGEL PETER	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-29 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Garde (Published PCT application publication No. WO 92/08186)(submitted by applicant) in view of Shridhar (patent No. 5,381,360).

3. Garde taught the invention as claimed including a data processing ("DP") system comprising (As per claims 1,3,22,23,28,29 and method steps of claims 26,27):

4. Mapping circuitry for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values(e.g., see page 5), said circuitry comprising:

A first candidate output value producing unit (22) connected for receiving the input value and operable to produce a first candidate output value that differs by a first offset value from the received input value (e.g., see page 5)[first offset is M];

A second candidate output value producing unit (28) connected for receiving the input value and operable, , to produce a second candidate output value that differs by a second offset value [M-L] from the received input value, the first and second offset values being such that a difference between them is equal to a difference between

respective output-range limit values defining the limits of the pre-selected output-value range (e.g., see page 5) and such that, for any said input value within the pre-selected input-value range, one of the first and second candidate output values is within the pre-selected output-value range and the other of those two values is outside that range (e.g., see pages 5 and 11); and

An in-range value determining unit (comparator, 50) which determines which one of the first and second candidate output values is within the preselected output-value range; and and output value selection unit (multiplexer, 32) which selects as the corresponding output value that one of the first and second candidate output values which is determined to be within the output-value range (e.g., see pages 5,10, and figs. 3, 4, 5).

5. Garde did not expressly detail (claims 1,3,22,23,26,27,28,29) that the second candidate value and the first candidate values were produced during the operation of the first candidate value producing unit. Shrihar however taught plural candidate output value producing units (1872,1870 in fig. 1) that each produce the first and second output values at the same time (e.g., see col. 7, lines 48-67 and col. 10, lines 11-66).

6. It would have been obvious to one of ordinary skill to combine the teachings of Garde and Shrihar. Both references were directed toward the problems of producing plural data values that are preselect offset from each other from a first value and selecting the one of the two values that are within a pre-selected range of values where the values represent address values. One of ordinary skill would have been motivated to incorporate the Shrihar teachings plural candidate producing units that produce the

candidate values in parallel at least to provide the values in less time. Also the incorporation of the Shirhar teachings into the Garde system would have yielded a predictable result.

7. As to the further limitations of claim 22,23 Shirhar taught an addressing system used in DSPs (e.g,. see col. 1, lines 45-60). Systems that incorporate DSPs are well known to comprise an instruction issuing unit which issues instructions; at least one instruction executing unit which executes the issued instructions a register file, having a plurality of physical registers and mapping circuitry. Shirhar also taught a system that maps an input value within a preselected range of allowable input values to a corresponding output value within a preselected range of allowable output values the input value being a logical register identifier specified by one of the instructions and the output value being a physical register identifier for identifying one of the physical registers within the register file that corresponds to the specified logical register identifier; (e.g., see col. 5, lines 28-67 and col. 8 lines 1-67 and col. 10, lines 11-26).

8. As to the further limitations of claims 2,3 Since the Shirar system provided the parallel operation of the candidate output value producing units then is would have been obvious to one of ordinary skill that the production of the output values is within a preselected output-value range during operation of both the first and second candidate value producing units to produce the first and second output values (e.g., see figs. 1,2 and col. 7, line 48-col. 8, line 67).

9. As per claim 4, Shrihar taught a taught input range determining unit connected for receiving the input value and operable to determine whether the input value is within

the preselected input-value range; and third candidate output value producing unit which produces a third candidate output value wherein the output value selection unit is operable when the input value is outside the preselected input-output range to select as the corresponding output value the third candidate output value (e.g., see fig. 1 and col. 4, lines 33-67 and col. 7, line 48-col. 8, line 67).

10. As per claims 5, Shrihar taught the third candidate output value producing unit is connected for receiving the input value and the third candidate value is dependent of on the input value (e.g., see fig. 1) [the Yau and Xau receive the input value and the modulo logics 1872 and 1870 produce the output values].

11. As per claim 6, Garde taught the ouput equals I+M+L or I+M-L. In the situation where M equals L the input would equaled the output (e.g., see fig. 3 and page 5).

12. As per claim 7, Shrihar taught the input range determining unit is operable to determine whether the input value is outside the preselected input-output range during operation of one or both of the first and second candidate value producing units to produce the first and second candidate output values (e;g., see fig. 1 and col. 7, line 48-col. 8, line 68)[input units 1812 and 1814 are connected and operate for determination of the input values during the operation of both the first and second candidate value producing units].

13. As per claim 8, Shrihar taught the third candidate output value producing unit is operable to produce the third candidate output value during operation of one or both of the first and second candidate value producing units to produce the first ant second candidate output values (e.g., see fig. 1).

14. As per claim 9, Garde taught at least one of the output-range limit values is variable during operation of the circuitry (the M register and the I register and the Length register is changed during the operation of the system and is used to indicate the output range)(e.g., see page 8).

15. As per claim 10, Garde taught the span of the pre-selected output-value range is greater than the span of the preselected input-value range (e.g., see page 10)[using the output equal I+M-L or I+M+L provides for the output having a wider range than the input].

16. As per claims 11,12 Garde taught the input range determining unit is operable to determine whether the input value is outside the preselected input-value range by producing a detection value that differs by a third offset value from the received input value, and detecting when a predetermined bit of the detection value has a predetermined logic value (e.g., see page 10). The Garde system produces a detection offset value "M". The value is set independence upon an input-range limit value defining one of the limits of the predetermined input-value value (e.g. see page 7). Where M can be positive or negative and therefore the detection is independent on the sign bit of the M value (e.g., see page 12).

17. As per claim 13,14 Garde taught the predetermined bit is the most significant bit of the produced detection value. (e.g., see page 12) Garde taught a system that operates when M is positive or negative and therefore determines the sign bit of M to determine the output value which would have been the most significant bit of the M value in at least one implementation.

18. As per claim 15, Garde taught the selectively varying the first and second offset values during the operation of the circuitry, whilst maintaining the difference between them (e.g., see page 8) [the increment value M is loaded or varied].

19. As per claim 16, Garde taught the in-range value determining unit is operable to produce a detection value that differs by an in-range offset value from the received input value, and to determine that the in-range output value is the first candidate output value when a preselected bit of the produced detection value has a first logic value and that the in-range candidate output value as the second candidate output value when the bits has a second logic value (e.g., see fig. 3) [candidate value is I+M-L if M is positive where the sign bit would have a first logic value and the candidate value is I+M+L if M is negative where the sign bit would have a second logic value].

20. As per claim 17, Garde taught the in-range offset value differs from the first offset value by one of the output-range limit values and differs from the second offset value by the other of the output-range limit values. [the in range offset value M differs from the first offset by L and from the second offset by minus L see fig. 3].

21. As per claim 18, Garde taught an offset varying unit operable selectively to vary the first and second offset values during operation of the circuitry, whilst maintaing the difference between them, and wherein the offset varying unit also varies the in-range offset value when the first and second offset values are varied so between the first and n-range offset value when the first and second offset values are varied so as to leave unchanged the respective difference between the first and in-range offset values and between the second and in-range offset values.[by changing the value of M the offset

values are changed without changing the difference between the offsets (e.g,. see fig. 3)].

22. As per claim 19, Garde taught the in range offset value is dependent upon an input-range limit value defining the limits of the pre-selected input-value range (e.g., see page 10). Garde produces a detection offset value "M". The value is set independence upon an input-range limit value defining one of the limits of the predetermined input-value value (e.g. see page 7). Where M can be positive or negative and therefore the detection is independent on the sign bit of the M value (e.g., see page 12).

23. As per claim 20, Garde taught the detection value is produced by adding the in-range offset value to the received input value (e.g., see fig. 3)[M is added to I].

24. As per claim 21, Garde taught the preselected bit is the most significant bit (e.g., see page 12) Garde taught a system that operates when M is positive or negative and therefore determines the sign bit of M to determine the output value which would have been the most significant bit of the M value in at least one implementation.

25. As per claim 24, Shridhar taught the register file comprises a dynamically-named region and mapping-circuitry output values within the predetermined output-value range provide the physical register identifiers of those physical registers within the dynamically-named region (e.g., see col. 8, lines 1-67).

26. As per claim 25, Garde taught register file comprises statically-named region and mapping-circuitry output values outside the predetermined output-value range provide the physical register identifiers of those physical registers within the statically-named region (e.g. see fig. 3 and page 11).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Holmqvist disclosed a modulo address generator for generating an updated address (e.g., see abstract).

Roesgen (patent No. 4,800,524) disclosed modulo address generator (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER